

AMENDMENT TO THE CLAIMS:

This listing of the claims replaces all prior versions, and listings, of claims in the application. Claims 18 and 19 are added.

1 1. (Original) A host platform/PVDM (packet voice data module) interface
2 where the packet module includes at least one on-board DSP compatible with one particular
3 host parallel bus protocol of a set of parallel bus protocols, said interface comprising:
4 a parallel bus coupled to the host ports of the DSP;
5 a non-volatile memory holding information indicating which one of the
6 parallel bus protocols is utilized by the on-board DSP;
7 a serial bus coupled to the non-volatile memory for reading the information
8 held on the non-volatile memory; and
9 termination logic, capable of implementing each protocol in the set of parallel
10 bus protocols, for reading the information from the non-volatile memory and implementing
11 the parallel bus protocol, identified by the non-volatile memory, utilized by the on-board
12 DSP.

1 2. (Original) The interface of claim 1 further comprising:
2 a test and emulation bus for allowing diagnostic testing of on-board
3 components.

1 3. (Original) The interface of claim 2 further comprising:
2 multiple time-division multiplexed buses coupled to the on-board DSP.

1 4. (Original) The interface of claim 1 where the PVDM includes a plurality of
2 on-board DSPs, the interface further comprising:
3 a like plurality of DSP chip selects for selecting a particular one of the
4 plurality of on-board DSPs to respond to the parallel bus; and
5 a hardware chip select for communication with a device on board the PVDM
6 that provides special functionality.

1 5. (Original) The interface of claim 1 with said non-volatile memory further
2 holding digital signature information utilized by the host for unambiguous module
3 identification.

1 6. (Original) A method for interfacing a host platform and a PVDM (packet
2 voice data module), where the packet module includes at least one on-board DSP (digital
3 signal processor), which is compatible with one particular host parallel bus protocol out of a
4 set of parallel bus protocols that can be implemented by host platform, and where the PVDM
5 includes a non-volatile memory holding identification information identifying the type of on-
6 board DSP, said method, with a configurable parallel bus and serial bus coupling the host
7 platform and PVDM, said method, performed by host processor on the host platform,
8 comprising the steps of:
9 reading the non-volatile memory over the serial bus to access the identification
10 information to identify a particular parallel bus protocol, out of the set of parallel bus
11 protocols, that is compatible with the on-board DSP; and
12 configuring the parallel bus to implement the particular parallel bus protocol
13 to communicate with the on-board DSP.

1 7. (Original) The method of claim 6, where the non-volatile memory holds
2 digital signature information, and further comprising the step of:
3 reading the digital signature information; and
4 unambiguously identifying the PVDM based on the digital signature
5 information.

1 8. (Original) The method of claim 6 where a dedicated hardware chip select
2 line couples the host platform to the PVDM and where the PVDM includes a non-DSP
3 module, said method further comprising the step of:
4 utilizing the hardware chip select line to select the non-DSP module without
5 disturbing DSP chip selecting functionality.

1 9. (Original) The method of claim 6 where said step of configuring the
2 parallel bus further comprises the steps of:
3 selecting the function of a particular DMA control line of the bus to be
4 compatible with the DMA operation of an identified on-board DSP.

1 10. (Original) A system for interfacing a host platform and a PVDM (packet
2 voice data module), where the packet module includes at least one on-board DSP (digital
3 signal processor), which is compatible with one particular host parallel bus protocol out of a
4 set of parallel bus protocols that can be implemented by host platform, and where the PVDM
5 includes a non-volatile memory holding identification information identifying the type of on-
6 board DSP, with a configurable parallel bus and serial bus coupling the host platform and
7 PVDM, said system comprising:
8 means for reading the non-volatile memory over the serial bus to access the
9 identification information to identify a particular parallel bus protocol, out of the set of
10 parallel bus protocols, that is compatible with the on-board DSP; and
11 means for configuring the parallel bus to implement the particular parallel bus
12 protocol to communicate with the on-board DSP.

1 11. (Original) The system of claim 10, where the non-volatile memory holds
2 digital signature information, and further comprising:
3 means for reading the digital signature information; and
4 means for unambiguously identifying the PVDM based on the digital signature
5 information.

1 12. (Original) The system of claim 10 where a dedicated hardware chip select
2 line couples the host platform to the PVDM and where the PVDM includes a non-DSP
3 module, said system further comprising:
4 means for utilizing the hardware chip select line to select the non-DSP module
5 without disturbing DSP chip selecting functionality.

1 13. (Original) The system of claim 10 where said means for configuring the
2 parallel bus further comprises:
3 means for selecting the function of a particular DMA control line of the bus to
4 be compatible with the DMA operation of an identified on-board DSP.

1 14. (Original) A computer program product, executed by a host processor, for
2 interfacing a host platform and a PVDM (packet voice data module), where the packet
3 module includes at least one on-board DSP (digital signal processor), which is compatible
4 with one particular host parallel bus protocol out of a set of parallel bus protocols that can be
5 implemented by host platform, and where the PVDM includes a non-volatile memory holding
6 identification information identifying the type of on-board DSP, with a configurable parallel
7 bus and serial bus coupling the host platform and PVDM, said computer program product
8 comprising:

9 a computer usable medium having computer readable program code physically
10 embodied therein, said computer program product further comprising:

11 computer readable program code executed by the host processor for reading
12 the non-volatile memory over the serial bus to access the identification information to
13 identify a particular parallel bus protocol, out of the set of parallel bus protocols, that is
14 compatible with the on-board DSP; and

15 computer readable program code executed by the host processor for
16 configuring the parallel bus to implement the particular parallel bus protocol to communicate
17 with the on-board DSP.

1 15. (Original) The computer program product of claim 14, where the non-
2 volatile memory holds digital signature information, and further comprising:

3 computer readable program code executed by the host processor for reading
4 the digital signature information; and

5 computer readable program code executed by the host processor for
6 unambiguously identifying the PVDM based on the digital signature information.

1 16. (Original) The computer program product of claim 14 where a dedicated
2 hardware chip select line couples the host platform to the PVDM and where the PVDM
3 includes a non-DSP module, said system further comprising:
4 computer readable program code executed by the host processor for utilizing
5 the hardware chip select line to select the non-DSP module without disturbing DSP chip
6 selecting functionality.

1 17. (Original) The computer program product of claim 14 where said means
2 for configuring the parallel bus further comprises:
3 computer readable program code executed by the host processor for selecting
4 the function of a particular DMA control line of the bus to be compatible with the DMA
5 operation of an identified on-board DSP.

1 18. (New) A PVDM (packet voice data module) to be coupled to a slot on a
2 motherboard, where the PVDM includes at least one on-board DSP compatible with one
3 particular host parallel bus protocol of a set of parallel bus protocols, said PVDM comprising:
4 a parallel bus interface coupled to the host ports of the DSP, with the parallel
5 bus interface adapted to be coupled to a parallel bus on the motherboard;
6 a non-volatile memory holding information indicating which one of the
7 parallel bus protocols is utilized by the on-board DSP;
8 a serial bus interface coupled to the non-volatile memory to allow a processor
9 on the motherboard to read the information held on the non-volatile memory so that
10 termination logic on the motherboard, capable of implementing each protocol in the set of
11 parallel bus protocols, can read the information from the non-volatile memory and implement
12 the parallel bus protocol, identified by the non-volatile memory, utilized by the on-board
13 DSP.

1 19. (New) A host platform having a motherboard including a processor and a
2 slot for accepting a PVDM (packet voice data module) to be coupled to a slot on a
3 motherboard, where the PVDM includes at least one on-board DSP compatible with one
4 particular host parallel bus protocol of a set of parallel bus protocols and also includes a non-

5 volatile memory holding information indicating which one of the parallel bus protocols is
6 utilized by the on-board DSP, said host platform comprising:
7 a parallel bus coupled to the host ports of the DSP, with the parallel bus
8 interface adapted to be coupled to a parallel bus on the motherboard;
9 a serial bus interface adapted to be coupled to the non-volatile memory on the
10 PVDM to allow the processor on the motherboard to read the information held on the non-
11 volatile memory so that termination logic on the motherboard, capable of implementing each
12 protocol in the set of parallel bus protocols, can read the information from the non-volatile
13 memory and implement the parallel bus protocol, identified by the non-volatile memory,
14 utilized by the on-board DSP.